National Semiconductor

August 2003

LM2619MTC
500mA Step-Down DC-DC Converter

General Description

The LM2619MTC step down DC-DC converter is optimized for powering circuits from a single Lithium-Ion cell. It steps down an input voltage of 2.8V to 5.5V to an output of 1.5V to 3.6V at up to 500mA. Output voltage is set using resistor feedback dividers.

The device offers three modes for mobile phones and similar portable applications. Fixed-frequency PWM mode minimizes RF interference. A SYNC input allows synchronizing the switching frequency in a range of 500kHz to 1MHz. Low current hysteretic PFM mode reduces quiescent current to 160µA (typ). Shutdown mode turns the device off and reduces battery consumption to 0.02µA (typ.).

Current limit and thermal shutdown features protect the device and system during fault conditions.

The LM2619MTC is available in a 14 pin TSSOP package. A high switching frequency (600kHz) allows use of tiny surface-mount components.

The device features external compensation to tailor the response to a wide range of operating conditions.

Key Specifications

- Operates from a single LiION cell (2.8V to 5.5V)
- Output voltage range of 1.5V to 3.6V
- ±2% DC feedback voltage precision
- 500mA maximum load capability
- 600µA typ PWM mode quiescent current
- 0.02µA typ shutdown current
- 600kHz PWM switching frequency
- SYNC input for PWM mode frequency synchronization from 500kHz to 1MHz
- High efficiency (Up to 95%) in PWM mode from internal synchronous rectification
- 100% Maximum Duty Cycle for Lowest Dropout

Features

- 14-pin TSSOP package
- Uses small ceramic capacitors
- 5mV typ PWM mode output voltage ripple(C_{OUT} = 22µF)
- Internal soft start
- Current overload protection
- Thermal Shutdown
- External compensation

Applications

- Mobile Phones
- Hand-Held Radios
- RF PC Cards
- Wireless LAN Cards

Typical Application Circuits

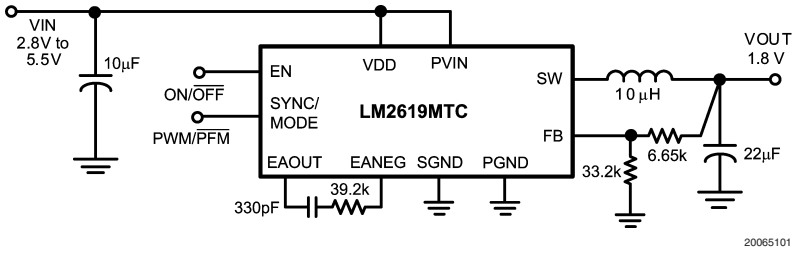


FIGURE 1. Typical Circuit for 1.8V Output Voltage

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Typical Application Circuits (Continued)

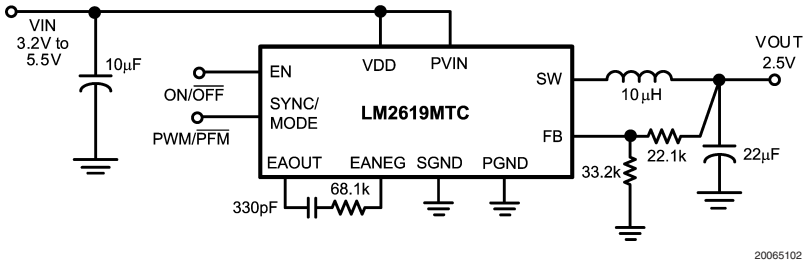


FIGURE 2. Typical Circuit for 2.5V Output Voltage

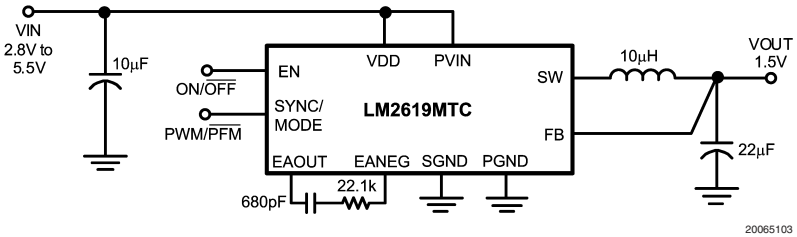
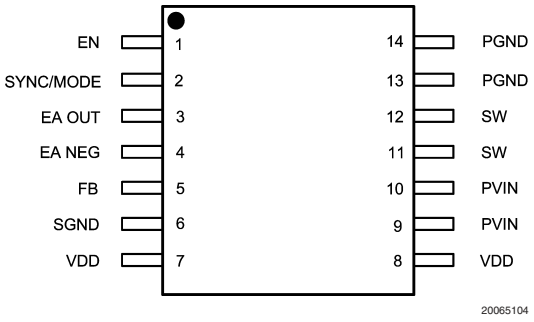


FIGURE 3. Typical Circuit for 1.5V Output Voltage

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Connection Diagrams

14-Pin TSSOP



Top View

Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM2619MTC	TSSOP - 14	MTC14	94 Rail
LM2619MTCX		MTC14	2500 Tape and Reel

Pin Description

Pin Number	Pin Name	Function
1	EN	Enable Input. Set this Schmitt trigger digital input high for normal operation. For shutdown, set low. Set EN low during system power-up and other low supply voltage conditions. (See *Shutdown Mode* in the *Device Information* section.)
2	SYNC/MODE	Synchronization Input. Use this digital input for frequency selection or modulation control. Set: SYNC/MODE = high for low-noise 600kHz PWM mode SYNC/MODE = low for low-current PFM mode SYNC/MODE = a 500kHz–1MHz external clock for synchronization in PWM mode. (See *Synchronization and Operating Modes* in the *Device Information* section.)
3	EAOUT	Output of error amplifier.
4	EANEG	Inverting Input of Error Amplifier.
5	FB	Feedback Analog Input.
6	SGND	Analog and Control Ground.
7,8	VDD	Analog Supply Input. If board layout is not optimum, an optional 0.1µF ceramic capacitor is suggested from this pin to SGND.
9,10	PVIN	Power Supply Voltage Input to the internal PFET switch. Connect to the input filter capacitor.
11,12	SW	Switching Node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the max Switch Peak Current Limit of the LM2619MTC.
13,14	PGND	Power Ground.

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

PVIN, VDD to SGND	−0.2V to +6V
PGND to SGND, PVIN to VDD	−0.2V to +0.2V
EN, EAOUT, EANEG, SYNC/MODE to SGND	−0.2V to +6V
FB, SW	(GND −0.2V) to (VDD +0.2V)
Storage Temperature Range	−45˚C to +150˚C
Lead Temperature (Soldering, 10 sec.)	300˚C
Junction Temperature (Note 2)	+125˚C
Ambient Temperature Range	-25˚C to 85˚C
Minimum ESD Rating (Human Body Model, C = 100 pF, R = 1.5 kΩ)	±2 kV
Thermal Resistance (θ_{JA}) (Note 3)	110˚C/W

Electrical Characteristics

Specifications with standard typeface are for T_A = 25˚C, and those in **boldface type** apply over the full **Operating Junction Temperature Range** of T_J = −25˚C to +125˚C. Unless otherwise specified, PVIN = VDD = EN = SYNC/MODE = 3.6V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage Range	PVIN = VDD = V_{IN} (Note 4)	2.8	3.6	5.5	V
V_{FB}	Feedback Voltage		**1.470**	1.50	**1.530**	V
V_{HYST}	PFM Comparator Hysteresis Voltage	PFM Mode (SYNC/MODE = 0V) (Note 5)		29		mV
I_{SHDN}	Shutdown Supply Current	VIN = 3.6V, EN = 0V		0.02	0.3	µA
I_{Q1_PWM}	DC Bias Current into VDD	SYNC/MODE = VIN FB = 2V		600	**725**	µA
I_{Q2_PFM}		SYNC/MODE = 0V FB = 2V		160	**195**	µA
$R_{DSON\ (P)}$	Pin-Pin Resistance for P FET	(Note 6)		500	630	mΩ
$R_{DSON\ (N)}$	Pin-Pin Resistance for N FET	(Note 6)		420	550	mΩ
$R_{DSON\ (TC)}$	FET Resistance Temperature Coefficient			0.5		%/C
I_{LIM}	Switch Peak Current Limit (Note 7)		**620**	850	**1100**	mA
V_{IH}	Logic High Input, EN, SYNC/MODE			0.95	**1.3**	V
V_{IL}	Logic Low Input, EN, SYNC/MODE		**0.4**	0.80		V
F_{SYNC}	SYNC/MODE Clock Frequency Range	(Note 8)	**500**		**1000**	kHz
F_{OSC}	Internal Oscillator Frequency	PWM Mode	468	640	800	kHz
T_{min}	Minimum ON-Time of PFET Switch in PWM Mode			200		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but device specifications may not be guaranteed. For guaranteed specifications and associated test conditions, see the Min and Max limits and Conditions in the Electrical Characteristics table. Typical (typ) specifications are mean or average values at 25˚C and are not guaranteed.

Note 2: Thermal shutdown will occur if the junction temperature exceeds 150˚C.

Note 3: Thermal resistance specified with 4" x 3" JEDEC (2 layer 2 oz Cu.) board.

Note 4: The LM2619MTC is designed for mobile phone applications where turn-on after system power-up is controlled by the system controller. Thus, it should be kept in shutdown by holding the EN pin low until the input voltage exceeds 2.8V.

Note 5: The hysteresis voltage is the minimum voltage swing on the FB pin that causes the internal feedback and control circuitry to turn the internal PFET switch on and then off during PFM mode. When resistor dividers are used like in the operating circuit of *Figure 4*, the hysteresis at the output will be the value of the hysteresis at the feedback pin times the resistor divider ratio. In this case, 24mV (typ) x ((46.4k + 33.2k)/33.2k).

Note 6: R_{DSON} is specified by having the two PVIN pins connected together,two PGND pins connected together and the two SW pins connected together.

Note 7: Current limit is built-in, fixed, and not adjustable. If the current limit is reached while the voltage at the FB pin is pulled below 0.7V, the internal PFET switch turns off for 2.5µs to allow the inductor current to diminish.

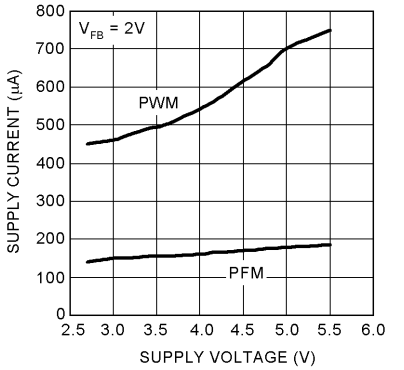
Note 8: SYNC driven with an external clock switching between V_{IN} and GND. When an external clock is present at SYNC; the IC is forced to be in PWM mode at the external clock frequency. The LM2619MTC synchronizes to the rising edge of the external clock.

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Typical Performance Characteristics

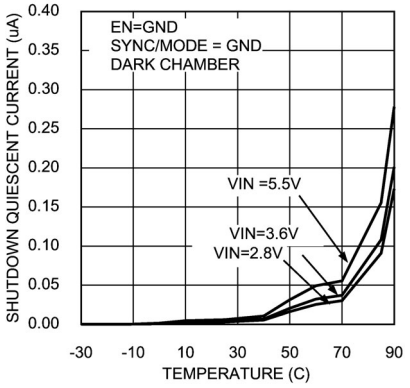
LM2619MTC, Circuit of *Figure 3*, V_{IN} = 3.6V, T_A = 25˚C, unless otherwise noted.

Quiescent Supply Current vs Supply Voltage



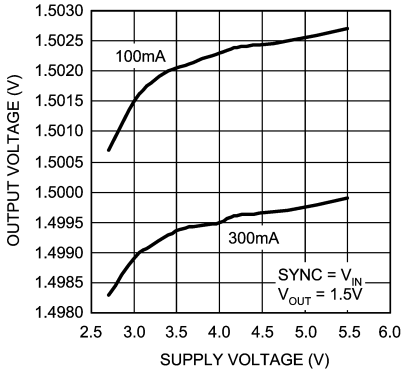
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Shutdown Quiescent Current vs Temperature (Circuit in *Figure 3*)



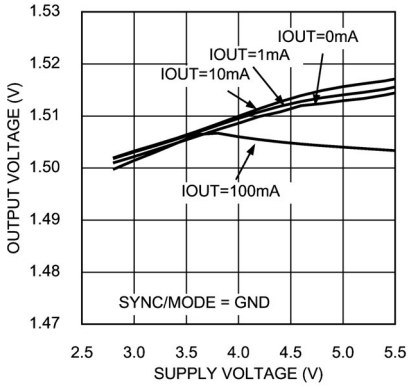
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Output Voltage vs Supply Voltage (V_{OUT} = 1.5V, PWM MODE)



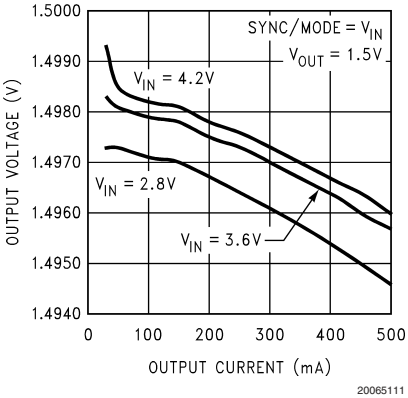
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Output Voltage vs Supply Voltage (V_{OUT} = 1.5V, PFM MODE)



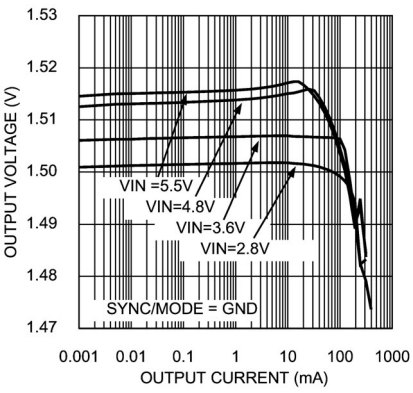
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Output Voltage vs Output Current (V_{OUT} = 1.5V, PWM MODE)



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Output Voltage vs Output Current (V_{OUT} = 1.5V, PFM MODE)

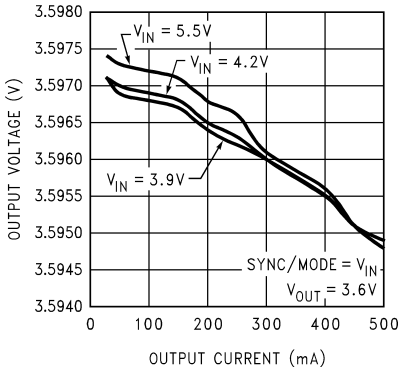


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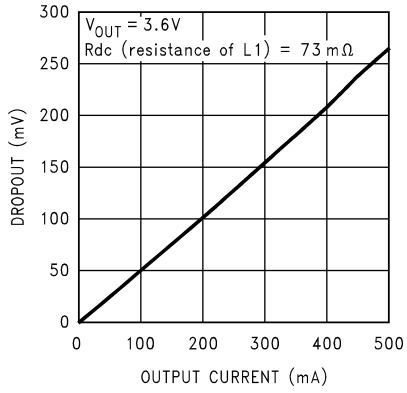
Typical Performance Characteristics LM2619MTC, Circuit of *Figure 3*, V_{IN} = 3.6V, T_A = 25˚C, unless otherwise noted. (Continued)

Output Voltage vs Output Current (V_{OUT} = 3.6V, PWM MODE) (Circuit in *Figure 4*)



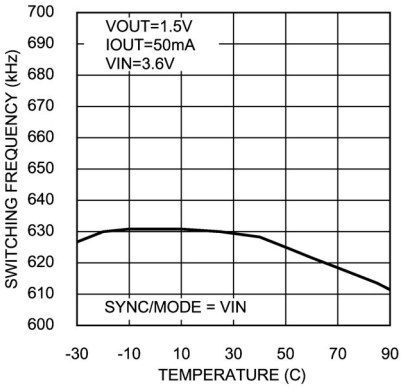
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Dropout Voltage vs Output Current (V_{OUT} = 3.6V, PWM MODE) (Circuit in *Figure 4*)



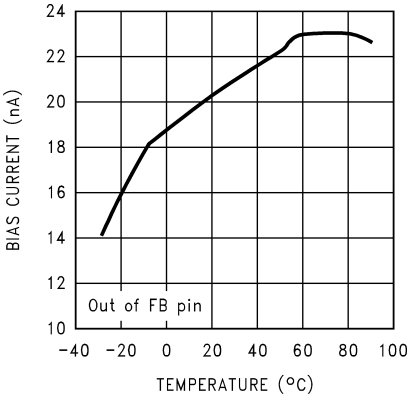
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Switching Frequency vs Temperature (Circuit in *Figure 3*, PWM MODE)



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Feedback Bias Current vs Temperature (Circuit in *Figure 3*)

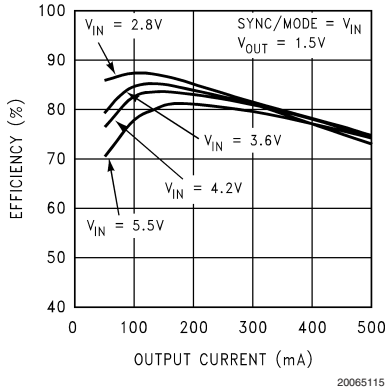


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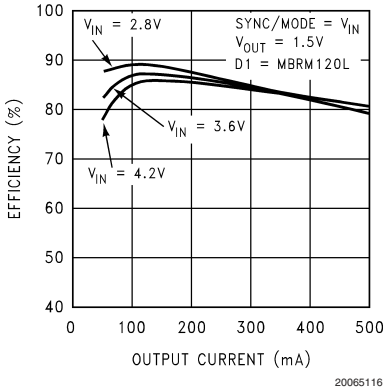
Typical Performance Characteristics LM2619MTC, Circuit of *Figure 3*, V_{IN} = 3.6V, T_A = 25˚C, unless otherwise noted. (Continued)

Efficiency vs Output Current (V_{OUT} = 1.5V, PWM MODE)



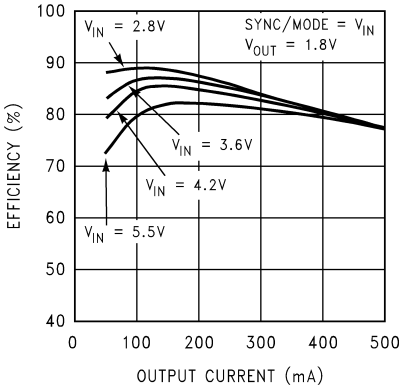
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Efficiency vs Output Current (V_{OUT} = 1.5V, PWM MODE, with Diode)



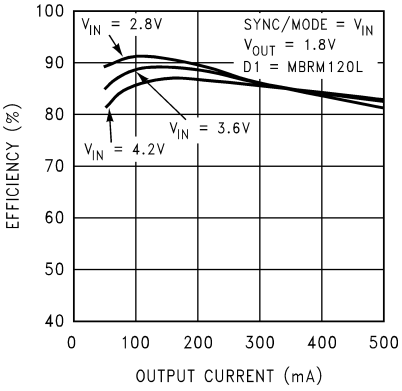
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Efficiency vs Output Current (V_{OUT} = 1.8V, PWM MODE) (Circuit in *Figure 1*)



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Efficiency vs Output Current (V_{OUT} = 1.8V, PWM MODE, with Diode) (Circuit in *Figure 1*)



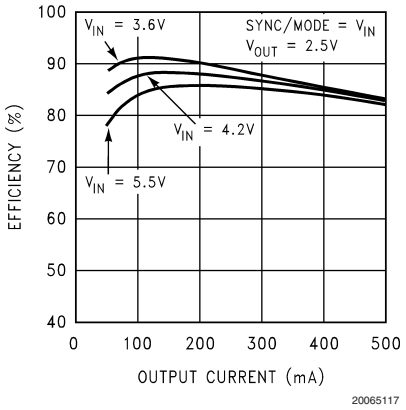
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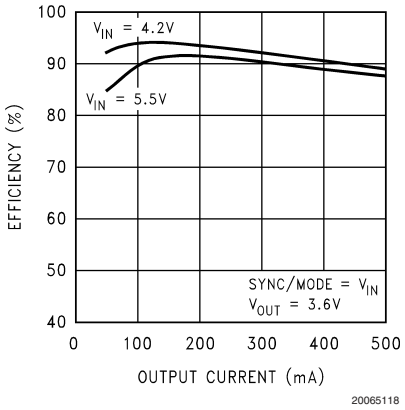
Typical Performance Characteristics

LM2619MTC, Circuit of *Figure 3*, V_{IN} = 3.6V, T_A = 25˚C, unless otherwise noted. (Continued)

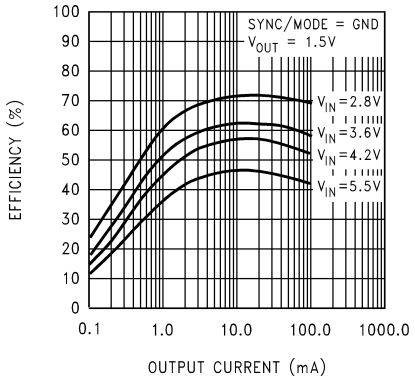
Efficiency vs Output Current (V_{OUT} = 2.5V, PWM MODE) (Circuit in *Figure 2*)



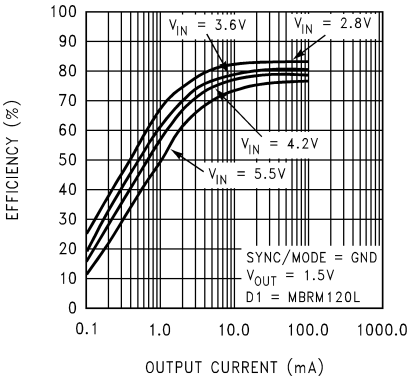
Efficiency vs Output Current (V_{OUT} = 3.6V, PWM MODE) (Circuit in *Figure 4*)



Efficiency vs Output Current (V_{OUT} = 1.5V, PFM MODE)



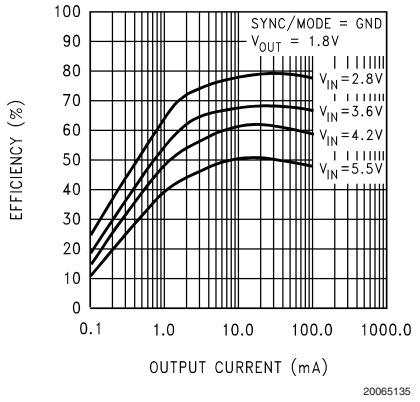
Efficiency vs Output Current (V_{OUT} = 1.5V, PFM MODE, with Diode)



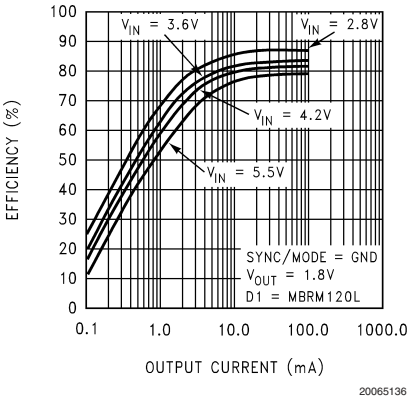
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Typical Performance Characteristics LM2619MTC, Circuit of *Figure 3*, V_{IN} = 3.6V, T_A = 25˚C, unless otherwise noted. (Continued)

Efficiency vs Output Current (V_{OUT} = 1.8V, PFM MODE) (Circuit in *Figure 1*)



Efficiency vs Output Current (V_{OUT} = 1.8V, PFM MODE, with Diode) (Circuit in *Figure 1*)



Device Information

The LM2619MTC is a simple, step-down DC-DC converter optimized for powering circuits in mobile phones, portable communicators, and similar battery powered RF devices. It is based on a current-mode buck architecture, with synchronous rectification in PWM mode for high efficiency. It is designed for a maximum load capability of 500mA in PWM mode. Maximum load range may vary from this depending on input voltage, output voltage and the inductor chosen.

The device has all three of the pin-selectable operating modes required for powering circuits in mobile phones and other sophisticated portable devices with complex power management needs. Fixed-frequency PWM operation offers full output current capability at high efficiency while minimizing interference with sensitive IF and data acquisition circuits. During standby operation, hysteretic PFM mode reduces quiescent current to 160µA typ. to maximize battery life. Shutdown mode turns the device off and reduces battery consumption to 0.02µA (typ).

DC PWM mode feedback voltage precision is ±2%. Efficiency is typically 93% for a 200mA load with 3.6V output, 4.2V input. The efficiency can be increased for lower output voltages like 1.5V,1.8V by using a schottky diode like MBRM120L as shown in *Figure 4*. PWM mode quiescent current is 600µA typ. The output voltage can be set from 1.5V to 3.6V by using external feedback resistors.

Additional features include soft-start, current overload protection, over voltage protection and thermal shutdown protection.

The LM2619MTC is constructed using a 14-pin TSSOP package. Use of a high switching frequency (600kHz) reduces the size of external components.

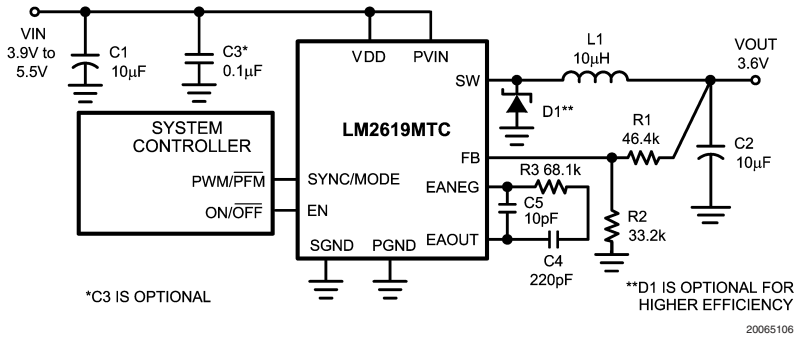


FIGURE 4. Typical Operating Circuit for 3.6V Output Voltage

CIRCUIT OPERATION

Referring to *Figure 4*, *Figure 5*, *Figure 6* and *Figure 7*, the LM2619MTC operates as follows. During the first part of each switching cycle, the control block in the LM2619MTC turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capaci-

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Device Information (Continued)

tor and load. The inductor limits the current to a ramp with a slope of $(V_{IN}–V_{OUT})/L$, by storing energy in a magnetic field. During the second part of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. In response, the inductor's magnetic field collapses, generating a voltage that forces current from ground through the synchronous rectifier to the output filter capacitor and load. As the stored energy is transferred back into the circuit and depleted, the inductor current ramps down with a slope of V_{OUT}/L. If the inductor current reaches zero before the next cycle, the synchronous rectifier is turned off to prevent current reversal. The output filter capacitor stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at SW to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

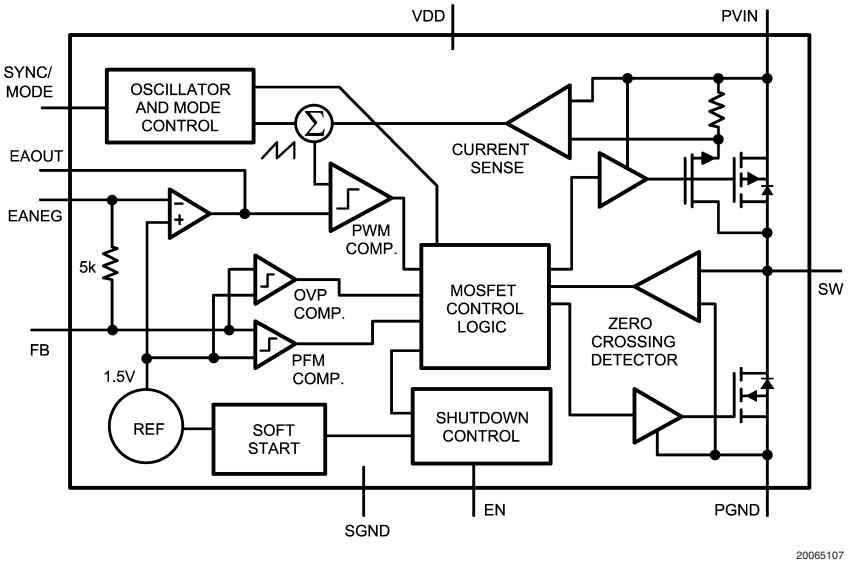


FIGURE 5. Simplified Functional Diagram

PWM OPERATION

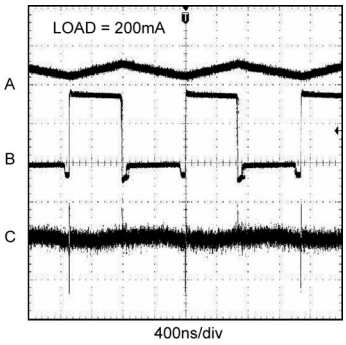
While in PWM (Pulse Width Modulation) mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. Energy per cycle is set by modulating the PFET switch on-time pulse-width to control the peak inductor current. This is done by comparing the signal from the current-sense amplifier with a slope compensated error signal from the voltage-feedback error amplifier. At the beginning of each cycle, the clock turns on the PFET switch, causing the inductor current to ramp up. When the current sense signal ramps past the error amplifier signal, the PWM comparator turns off the PFET switch and turns on the NFET synchronous rectifier, ending the first part of the cycle. If an increase in load pulls the output voltage down, the error amplifier output increases, which allows the inductor current to ramp higher before the comparator turns off the PFET. This increases the average current sent to the output and adjusts for the increase in the load.

Before going to the PWM comparator, the error signal is summed with a slope compensation ramp from the oscillator for stability of the current feedback loop. During the second part of the cycle, a zero crossing detector turns off the NFET synchronous rectifier if the inductor current ramps to zero. The minimum on time of the PFET in PWM mode is about 200ns.

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Device Information (Continued)

PWM Mode Switching Waveform



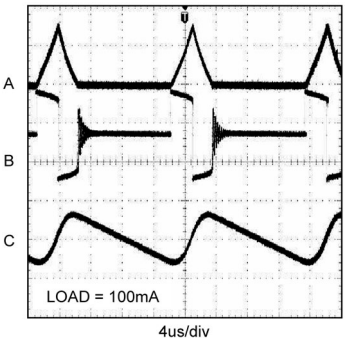
A: Inductor Current, 500mA/div

B: SW Pin, 2V/div

C: V_{OUT}, 10mV/div, AC Coupled

FIGURE 6.

PFM Mode Switching Waveform



A: Inductor Current, 500mA/div

B: SW Pin, 2V/div

C: V_{OUT}, 50mV/div, AC Coupled

FIGURE 7.

PFM OPERATION

Connecting the SYNC/MODE to SGND sets the LM2619MTC to hysteretic PFM operation. While in PFM (Pulse Frequency Modulation) mode, the output voltage is regulated by switching with a discrete energy per cycle and then modulating the cycle rate, or frequency, to control power to the load. This is done by using an error comparator to sense the output voltage. The device waits as the load discharges the output filter capacitor, until the output voltage drops below the lower threshold of the PFM error-comparator. Then the device initiates a cycle by turning on the PFET switch. This allows current to flow from the input, through the inductor to the output, charging the output filter capacitor. The PFET is turned off when the output voltage rises above the regulation threshold of the PFM error comparator. Thus, the output voltage ripple in PFM mode is proportional to the hysteresis of the error comparator.

In PFM mode, the device only switches as needed to service the load. This lowers current consumption by reducing power consumed during the switching action in the circuit, due to transition losses in the internal MOSFETs, gate drive currents, eddy current losses in the inductor, etc. It also improves light-load voltage regulation. During the second half of the cycle, the intrinsic body diode of the NFET synchronous rectifier conducts until the inductor current ramps to zero.

OPERATING MODE SELECTION

The LM2619MTC is designed for digital control of the operating modes by the system controller. This prevents the spurious switch over from low-noise PWM mode between transmission intervals in mobile phone applications that can occur in other products.

The SYNC/MODE digital input pin is used to select the operating mode. Setting SYNC/MODE high (above 1.3V) selects 600kHz current-mode PWM operation. PWM mode is optimized for low-noise, high-power operation for use when the load is active. Setting SYNC/MODE low (below 0.4V) selects hysteretic voltage-mode PFM operation. PFM mode is optimized for reducing power consumption and extending battery life when the load is in a low-power standby mode. In PFM mode, quiescent current into the V_{DD} pin is 160µA typ. In contrast, PWM mode V_{DD}-pin quiescent current is 600µA typ.

PWM operation is intended for use with loads of 50mA or more, when low noise operation is desired. Below 100mA, PFM operation can be used to allow precise regulation, and reduced current consumption. The LM2619MTC has an over-voltage feature that prevents the output voltage from rising too high, when the device is left in PWM mode under low-load conditions. See *Overvoltage Protection*, for more information.

Switch modes with the SYNC/MODE pin, using a signal with a slew rate faster than 5V/100µs. Use a comparator, Schmitt trigger or logic gate to drive the SYNC/MODE pin. Do not leave the pin floating or allow it to linger between thresholds. These measures will prevent output voltage errors in response to an indeterminate logic state. The LM2619MTC switches on each rising edge of SYNC. Ensure a minimum load to keep the output voltage in regulation when switching modes frequently.

FREQUENCY SYNCHRONIZATION

The SYNC/MODE input can also be used for frequency synchronization. During synchronization, the LM2619MTC initiates cycles on the rising edge of the clock. When synchronized to an external clock, it operates in PWM mode. The device can synchronize to a 50% duty-cycle clock over frequencies from 500kHz to 1MHz. If a different duty cycle is used other than 50% the range for acceptable duty cycles is 30% to 70%.

Use the following waveform and duty cycle guidelines when applying an external clock to the SYNC/MODE pin. Clock under/overshoot should be less than 100mV below GND or above V_{DD}. When applying noisy clock signals, especially sharp edged signals from a long cable during evaluation, terminate the cable at its characteristic impedance and add an RC filter to the SYNC pin, if necessary, to soften the slew rate and over/undershoot. Note that sharp edged signals

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Device Information (Continued)

from a pulse or function generator can develop under/overshoot as high as 10V at the end of an improperly terminated cable.

OVERVOLTAGE PROTECTION

The LM2619MTC has an over-voltage comparator that prevents the output voltage from rising too high when the device is left in PWM mode under low-load conditions. When the output voltage rises by about 100mV (*Figure 3*) over its regulation threshold, the OVP comparator inhibits PWM operation to skip pulses until the output voltage returns to the regulation threshold. When resistor dividers are used the OVP threshold at the output will be the value of the threshold at the feedback pin times the resistor divider ratio. In over voltage protection, output voltage and ripple will increase.

SHUTDOWN MODE

Setting the EN digital input pin low (<0.4V) places the LM2619MTC in a 0.02µA (typ) shutdown mode. During shutdown, the PFET switch, NFET synchronous rectifier, reference, control and bias circuitry of the LM2619MTC are turned off. Setting EN high enables normal operation. While turning on, soft start is activated.

EN should be set low to turn off the LM2619MTC during system power-up and undervoltage conditions when the supply is less than the 2.8V minimum operating voltage. The LM2619MTC is designed for compact portable applications, such as mobile phones. In such applications, the system controller determines power supply sequencing. Although the LM2619MTC is typically well behaved at low input voltages, this is not guaranteed.

INTERNAL SYNCHRONOUS RECTIFICATION

While in PWM mode, the LM2619MTC uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

The internal NFET synchronous rectifier is turned on during the inductor current down slope during the second part of each cycle. The synchronous rectifier is turned off prior to the next cycle, or when the inductor current ramps to zero at light loads. The NFET is designed to conduct through its intrinsic body diode during transient intervals before it turns on, eliminating the need for an external diode.

CURRENT LIMITING

A current limit feature allows the LM2619MTC to protect itself and external components during overload conditions. In PWM mode cycle-by-cycle current limit is normally used. If an excessive load pulls the voltage at the feedback pin down to approximately 0.7V, then the device switches to a timed current limit mode. In timed current limit mode the internal P-FET switch is turned off after the current comparator trips and the beginning of the next cycle is inhibited for 2.5µs to force the instantaneous inductor current to ramp down to a safe value. Timed current limit mode prevents the loss of current control seen in some products when the voltage at the feedback pin is pulled low in serious overload conditions.

DROPOUT CONSIDERATIONS

The LM2619MTC can be used to provide fixed output voltages by using external feedback resistors. The output voltage can be set from 1.5V to 3.6V. The internal reference voltage for the error amplifier is 1.5V. In cases where the output voltage is set to 2.5V or higher, the part will go into dropout or 100% duty cycle when the input voltage gets close to the set output voltage. Near dropout the on time of the P-FET may exceed one PWM clock cycle and cause higher ripple on the output for load currents greater than 300mA. This increased ripple will exist for a narrow range of input voltages close to the 100% duty cycle and once the input voltage goes down further the P-FET will be fully on. See *Setting the Output Voltage* in the *Application Information* section for further details.

In dropout conditions the output voltage is $V_{IN} - I_{OUT}$ (Rdc + $R_{DSON\ (P)}$) where Rdc is the series resistance of the inductor and $R_{DSON\ (P)}$ is the on resistance of the PFET.

Load Transient Response
(Circuit in *Figure 3*)

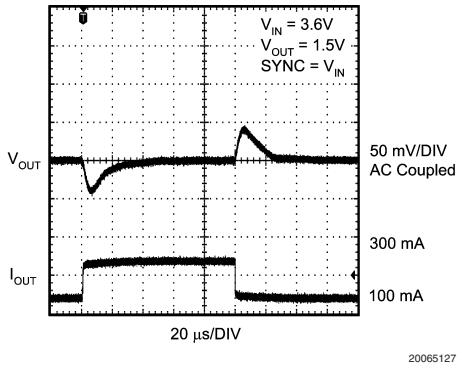


FIGURE 8.

Line Transient Response
(Circuit in *Figure 3*)

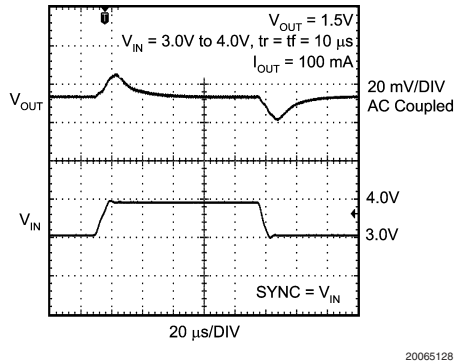


FIGURE 9.

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Device Information (Continued)

SOFT-START

The LM2619MTC has soft start to reduce current inrush during power-up and startup. This reduces stress on the LM2619MTC and external components. It also reduces startup transients on the power source. Soft start is implemented by ramping up the reference input to the error amplifier of the LM2619MTC to gradually increase the output voltage.

THERMAL SHUTDOWN PROTECTION

The LM2619MTC has a thermal shutdown protection function to protect itself from short-term misuse and overload conditions. When the junction temperature exceeds 150˚C the device turns off the output stage and when the temperature drops below 130˚C it initiates a soft start cycle. Prolonged operation in thermal shutdown conditions may damage the device and is considered bad practice.

Application Information

SETTING THE OUTPUT VOLTAGE

The LM2619MTC can be used with external feedback resistors to set the output voltage. Select the value of R2 to allow atleast 100 times the feedback pin bias current to flow through it.

$V_{OUT}= V_{FB}$ (1+R1/R2)

EXTERNAL COMPENSATION

The LM2619MTC uses external components connected to the EANEG and EAOUT pins to compensate the regulator (*Figure 4*). Typically, all that is required is a series connection of one capacitor (C4) and one resistor (R3). A capacitor (C5) can be connected across the EANEG and EAOUT pins to improve the noise immunity of the loop. C5 reacts with R3 to give a high frequency pole. C4 reacts with the high open loop gain of the error amplifier and the resistance at the EANEG pin to create the dominant pole for the system, while R3 and C4 react to create a zero in the frequency response. The pole rolls off the loop gain, to give a bandwidth somewhere between 10kHz and 50kHz, this avoids a 100kHz parasitic pole contributed by the current mode controller. Typical values in the 220pF to 1nF (C4) range are recommended to create a pole on the order of 10Hz or less.

The next dominant pole in the system is formed by the output capacitance (C2) and the parallel combination of the load resistance and the effective output resistance of the regulator. This combined resistance (Ro) is dominated by the small signal output resistance, which is typically in the range of 3Ω to 15Ω. The exact value of this resistance, and therefore this load pole depends on the steady state duty cycle and the internal ramp value. Ideally we want the zero formed by R3 and C4 to cancel this load pole, such that R3=RoC2/C4. Due to the large variation in Ro, this ideal case can only be achieved at one operating condition. Therefore a compromise of about 5Ω for Ro should be used to determine a starting value for R3. This value can then be optimized on the bench to give the best transient response to load changes, under all conditions. Typical values are 10pF for C5, 220pF to 1nF for C4 and 22K to 100K for R3.

A_O = 20000 , Open loop gain of error amplifier

R_f = 1 , Transresistance of output stage

M_c = 362000 A/s , Corrective ramp slope

D = VOUT/VIN , D' = 1-D , duty cycle

M_1 = (VIN - VOUT)/L1 , slope of current through inductor during PFET on time

$R_p = (R1 \parallel R2) + 5k\Omega$, effective resistance at inverting input of error amp

$R_o = (F \bullet L1) / (D' \bullet (M_c/M_1) + ½ - D)$

where R_o is the effective small signal output resistance of power stage

$f_{P1} = 1/(2 \bullet \pi \bullet A_O \bullet R_p \bullet C4)$, low frequency pole

$f_{P2} = 1/(2 \bullet \pi \bullet (Rload \parallel R_o) \bullet C2)$, pole due to Rload,Ro and C2

$f_{P3} = R_o/ (2 \bullet \pi \bullet L1)$, high frequency pole from current mode control

$f_{P4} = 1/(2 \bullet \pi \bullet R3 \bullet C5)$, high frequency pole due to R3 and C5

$f_{Z1} = 1/(2 \bullet \pi \bullet R3 \bullet C4)$, zero due to R3 and C4

α = R2/(R1+ R2)

$f_X = (\alpha \bullet (R_o \parallel Rload)/R_f)/(2 \bullet \pi \bullet R_p \bullet C4)$

where f_X gives the approximate crossover frequency.This equation for crossover frequency assumes that $f_{P2} = f_{Z1}$.

INDUCTOR SELECTION

Use a 10µH inductor with saturation current rating higher than the peak current rating of the device. The inductor's resistance should be less than 0.3Ω for good efficiency. *Table 1* lists suggested inductors and suppliers.

TABLE 1. Suggested Inductors and Their Suppliers

Part Number	Vendor	Phone	FAX
DO1608C-103	Coilcraft	847-639-6400	847-639-1469
ELL6SH100M	Panasonic	714-373-7366	714-373-7323
ELL6RH100M	Panasonic	714-373-7366	714-373-7323
CDRH5D18-100	Sumida	847-956-0666	847-956-0702
P0770.103T	Pulse	858-674-8100	858-674-8262

For low-cost applications, an unshielded inductor is suggested. For noise critical applications, a toroidal or shielded inductor should be used. A good practice is to lay out the board with footprints accommodating both types for design flexibility. This allows substitution of a low-noise shielded inductor, in the event that noise from low-cost unshielded models is unacceptable.

The saturation current rating is the current level beyond which an inductor loses its inductance. Different manufacturers specify the saturation current rating differently. Some specify saturation current point to be when inductor value falls 30% from its original value, others specify 10%. It is always better to look at the inductance versus current curve and make sure the inductor value doesn't fall below 30% at the peak current rating of the LM2619MTC. Beyond this rating, the inductor loses its ability to limit current through the PWM switch to a ramp. This can cause poor efficiency, regulation errors or stress to DC-DC converters like the

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Application Information (Continued)

LM2619MTC. Saturation occurs when the magnetic flux density from current through the windings of the inductor exceeds what the inductor's core material can support with a corresponding magnetic field.

CAPACITOR SELECTION

Use a 10µF ceramic input capacitor. Use X7R or X5R types, do not use Y5V.

Use of tantalum capacitors is not recommended.

Ceramic capacitors provide an optimal balance between small size, cost, reliability and performance for cell phones and similar applications. A 22µF ceramic output capacitor is recomended for applications that require increased tolerance to heavy load transients. A 10µF ceramic output capacitor can be used in applications where the worst case load transient step is less than 200mA. Use of a 10µF output capacitor trades off smaller size for an increase in output voltage ripple, and undershoot during load transients. *Table 2* lists suggested capacitors and suppliers.

The input filter capacitor supplies current to the PFET switch of the LM2619MTC in the first part of each cycle and reduces voltage ripple imposed on the input power source. The output filter capacitor smoothes out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

The ESR, or equivalent series resistance, of the filter capacitors is a major factor in voltage ripple.

TABLE 2. Suggested Capacitors and Their Suppliers

Model	Type	Vendor	Phone	FAX
C1, C2 (Input or Output Filter Capacitor)				
C2012X5ROJ106M	Ceramic	TDK	847-803-6100	847-803-6296
JMK212BJ106MG	Ceramic	Taiyo-Yuden	847-925-0888	847-925-0899
ECJ3YB0J106K	Ceramic	Panasonic	714-373-7366	714-373-7323
JMK325BJ226MM	Ceramic	Taiyo-Yuden	847-925-0888	847-925-0899
C3225X5RIA226M	Ceramic	TDK	847-803-6100	847-803-6296

BOARD LAYOUT CONSIDERATIONS

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability. Poor layout can also result in reflow problems leading to poor solder joints between the TSSOP package and board pads. Poor solder joints can result in erratic or degraded performance.

Good layout for the LM2619MTC can be implemented by following a few simple design rules.

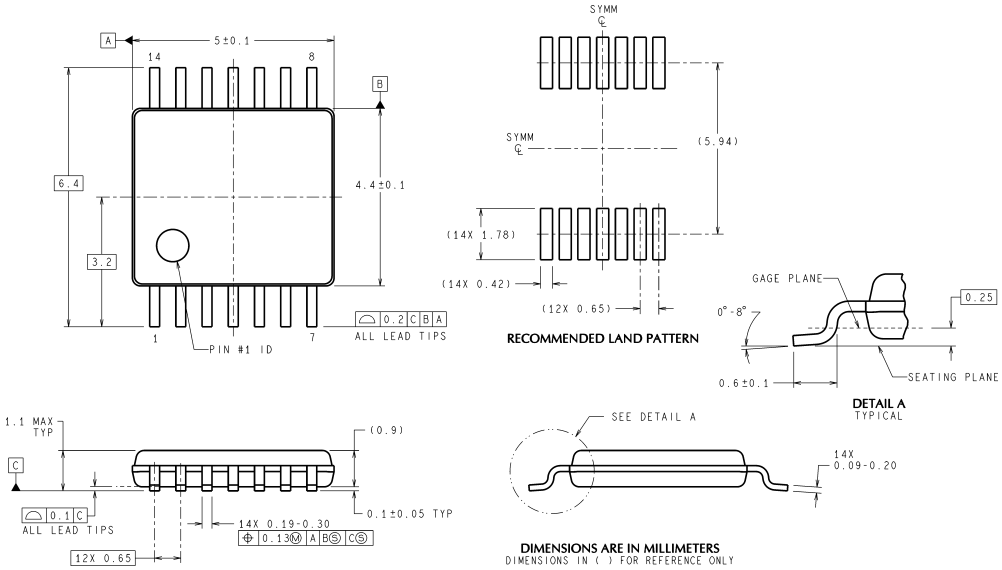
1. Follow the land pattern recomendation in the datasheet.
2. *Place the LM2619MTC, inductor and filter capacitors close together and make the traces short.* The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Place the capacitors and inductor within 0.2 in. (5 mm) of the LM2619MTC.
3. *Arrange the components so that the switching current loops curl in the same direction.* During the first half of each cycle, current flows from the input filter capacitor, through the LM2619MTC and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground, through the LM2619MTC by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
4. *Connect the ground pins of the LM2619MTC, and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then, connect this to the ground-plane (if one is used) with several vias.* This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LM2619MTC by giving it a low-impedance ground connection.
5. *Use wide traces between the power components and for power connections to the DC-DC converter circuit.* This reduces voltage errors caused by resistive losses across the traces.
6. *Connect the dual pins of the device together on the pcb for high efficiency.*
7. *Route noise sensitive traces, such as the voltage feedback path, away from noisy traces between the power components.* The voltage feedback trace must remain close to the LM2619MTC circuit and should be routed directly from V_{OUT} at the output capacitor and should be routed opposite to noise components. This reduces EMI radiated onto the DC-DC converter's own voltage feedback trace.
8. *Place noise sensitive circuitry, such as radio IF blocks, away from the DC-DC converter, CMOS digital blocks and other noisy circuitry.* Interference with noise-sensitive circuitry in the system can be reduced through distance.

In mobile phones, for example, a common practice is to place the DC-DC converter on one corner of the board, arrange the CMOS digital circuitry around it (since this also generates noise), and then place sensitive preamplifiers and IF stages on the diagonally opposing corner. Often, the sensitive circuitry is shielded with a metal pan and power to it is post-regulated to reduce conducted noise, using low-dropout linear regulators.

Book Extract End

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Physical Dimensions inches (millimeters) unless otherwise noted



MTC14 (Rev D)

NOTES: UNLESS OTHERWISE SPECIFIED

1. REFERENCE JEDEC REGISTRATION MO-153. VARIATION AB. REF NOTE 6. DATED 7/93

14-pin TSSOP
NS Package Number MTC14

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Notes

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